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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,419	04/01/2004	Judy M. Gehman	03-2477/L13.12-0258	1307

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EXAMINER	
VIDWAN, JASJIT S	

ART UNIT	PAPER NUMBER
2182	

MAIL DATE	DELIVERY MODE
06/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,419	GEHMAN ET AL.	
	Examiner	Art Unit	
	Jasjit S. Vidwan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 16-20* is/are pending in the application.

4a) Of the above claim(s) *8-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 are pending.

Claims 8-15 have been withdrawn from consideration as per response filed on 3/14/07.

Therefore, Claims 1-7 & 16-20 are being considered in this office action.

Applicant is respectfully advised to cancel any non-pending claims.

Election/Restrictions

1. Applicant's election of Claims 1-7 & 16-20 (Group I) in the reply filed on 03/14/07 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Specification

1. The disclosure is objected to because of the following informalities: Page 2 of the Applicant submitted specification reads "Present application is related to co-pending application Serial No: _____, filed _____, identified..." Applicant is encouraged to update any cross-references to the related application.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-7 & 16-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-7& 16-20 are rejected under 35 U.S.C. 101 because a "reusable software block" and "instantiating" are directed to software having abstract layers, which is software. Therefore, the above claims are program per se and therefore not statutory.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claims 2, 17 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In the above-mentioned claims, Applicant claims an abstraction layer comprising a "memory register" and "interrupt connections." However, it should be noted that the said claim is misdescription as a layer (software) can not contain physical memory registers or interrupt connections. For the purpose of timely prosecution of the current application, Examiner will construe the above limitations to read towards a "memory register location" and "interrupt configuration" to stay in line with other dependent claims.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-7 & 16-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Bowen, U.S. Publication No: 200/0100029 **[herein after Bowen]**.

7. **As per Claims 1 & 16**, Bowen teaches a system for instantiating multiple instances of a peripheral device within an integrated circuit using a single configurable code block **[see Page 12, Paragraph 0241-- *Bowen teaches a system of using the single code block coupled with a hardware tailored for a specific peripheral device to simply 'share' the block to allow using the dedicated software with greater flexibility for multiple functionality. This method of coding overcomes***

similar shortcoming of Applicant's prior art wherein the software block has to be reconfigured repeatedly [see Bowen, paragraph 0005] to use with a separate hardware device as is discussed in Applicant's "Background of the Invention"], the system comprising:

(a) Device hardware abstraction layer **[see Fig. 2, element 212, "Behavioral Synthesis"]** defining a configurable structure **[see Page 3, Paragraph 0053, "Behavioral description of the electronic system" – also see paragraph 0038]** for the peripheral device **[see Fig. 10, elements 1024, 1026, 1028, 1032, etc – also see Page 12, Paragraph 0238 for full list of peripheral devices]**

(b) Platform hardware abstraction layer **[see Fig. 2, element 214, RTL Synthesis]** adapted to configure the structure of each particular instantiation of the peripheral device via the device hardware abstraction layer **[see Page 7, Paragraphs 0144 & 0145 – "RTL synthesis optimizes the hardware description and maps it to a given technology.]**.

8. **As per Claim 2 & 17**, Bowen teaches a system wherein the device hardware abstraction layer comprises:

(a) Memory registers location **[see Paragraph 0054]** adapted to the configurable during initialization **[Paragraph 242, "OOP components are accessed at run-time through a component integration architecture]**

(b) Interrupt connections adapted to be configurable during initialization **[see Page 8, Paragraph 0170 – "The size of internal memory and of the stack or stacks can be set, the number and priorities of interrupts can be defined, an channels needed to communicate with external resources.."]**

9. **As per Claim 3 & 18**, Bowen teaches a system wherein the memory registers locations and the interrupt configurations define the structure of the peripheral device using variables **[see Paragraph 0062, "Variables are declared with explicit bit widths and the operators working on the variables work with an arbitrary precision."]**

10. **As per Claim 4, 5 & 19**, Bowen teaches a system wherein the platform hardware abstraction layer comprises a memory map of memory locations of the peripheral device corresponding to a particular

implementation of the peripheral device, the memory map adapted to replace the variables with unique memory locations for each instantiation **[see Paragraph 0315 – "Look up table (LUT)" with "resources" being the peripheral devices]**.

11. **As per Claim 6, 7 & 20**, Bowen teaches a system wherein the configurable structure of the peripheral device is defined in the device hardware abstraction layer using variables, the platform hardware abstraction layer comprising an interrupt configuration corresponding to interrupt connections for a particular implementation of the peripheral device, the interrupt configuration adapted to replace the variables with unique interrupt connections for each instantiation **[see Paragraph 0306]**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM HUYNH can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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implementation of the peripheral device, the memory map adapted to replace the variables with unique memory locations for each instantiation **[see Paragraph 0315 – "Look up table (LUT)" with "resources" being the peripheral devices]**.

11. **As per Claim 6, 7 & 20**, Bowen teaches a system wherein the configurable structure of the peripheral device is defined in the device hardware abstraction layer using variables, the platform hardware abstraction layer comprising an interrupt configuration corresponding to interrupt connections for a particular implementation of the peripheral device, the interrupt configuration adapted to replace the variables with unique interrupt connections for each instantiation **[see Paragraph 0306]**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

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KIM HUYNH
SUPERVISORY PATENT EXAMINER

5/29/07